WHAT IS CLAIMED IS:

1. A memory system on a chip, comprising:

a configurable memory having a first mode of operation wherein the configurable memory is configured as a cache and a second mode of operation wherein the configurable memory is configured as a local, non-cache memory, and

wherein a selection of any of the first mode of operation and the second mode of operation is capable of being overridden by an other selection of an other of the first mode of operation and the second mode of operation.

2. The memory system of claim 1, wherein the configurable memory is capable of having either the first mode of operation or the second mode of operation selected at a burn-in time.

3. The memory system of claim 2, wherein the first mode of operation or the second mode of operation is selected at the burn-in time using a fuse.

4. The memory system of claim 1, wherein the configurable memory is capable of having either the first

mode of operation or the second mode of operation selected at a power-up time.

5. The memory system of claim 4, wherein the first mode of operation or the second mode of operation is selected at the power-up time using an external signal

6. The memory system of claim 1, wherein the configurable memory is capable of having either the first mode of operation or the second mode of operation selected during a program execution.

7. The memory system of claim 6, wherein the first mode of operation or the second mode of operation is selected during the program execution based upon a value of a special configuration register.

8. The memory system of claim 6, wherein the first mode of operation or the second mode of operation is selected during the program execution based upon a value of an external signal.

9. The memory system of claim 6, wherein the first mode of operation or the second mode of operation is

selected during the program execution based upon a supplied address.

10. The memory system of claim 1, wherein the configurable memory is capable of having either the first mode of operation or the second mode of operation selected based upon a result of comparing a supplied address to a range of addresses.

11. The memory system of claim 10, wherein the range of addresses are determined at a burn-in time.

12. The memory system of claim 10, wherein the range of addresses are determined at a boot-up time.

13. The memory system of claim 10, wherein the range of addresses are determined dynamically.

14. The memory system of claim 10, further comprising a configuration register for storing the range of addresses.

15. The memory system of claim 1, wherein the configurable memory comprises:

a memory array; and

memory configuration logic for selecting the first mode of operation or the second mode of operation.

16. The memory system of claim 1, wherein the configurable memory is capable of selecting one of a local memory read mode and a local memory write mode in the first mode of operation and is further capable of selecting one of a cache read mode and a cache write mode in the second mode of operation.

17. The memory system of claim 1, wherein the selection may be overridden by the other selection dynamically.

18. The memory system of claim 1, wherein the configurable memory comprises a plurality of static random access memory cells.

19. The memory system of claim 1, wherein the configurable memory comprises a plurality of dynamic random access memory cells.

20. The memory system of claim 1, wherein the configurable memory is capable of being dynamically employed

as a sole memory serving the processor and as a portion of a larger, memory hierarchy.

21. The memory system of claim 1, wherein the first mode of operation and the second mode of operation are employed concurrently.

22. A memory system on a chip, comprising:

a configurable Random Access Memory (RAM) array having a first mode of operation wherein the configurable RAM array is configured as a local, non-cache memory and a second mode of operation wherein the configurable RAM array is configured as a cache, and

wherein the configurable RAM array has a memory portion for storing tag bits and data bits in a single logical line in the second mode of operation.

23. The memory system of claim 22, further comprising control logic for selectively providing direct access to the configurable RAM array as the local, non-cache memory in the first mode of operation and as the cache in the second mode of operation.

24. The memory system of claim 22, wherein the single logical line spans several physical macro cells.

25. The memory system of claim 22, further comprising:

tag match logic for determining a match between the stored tag bits and bits corresponding to a memory access; and

at least one multiplexer for selecting and outputting data corresponding to the memory access, when the match is determined.

26. A data storage system, comprising:

at least one microprocessor; and

a configurable memory, integrated with the at least one processor, for servicing the at least one microprocessor in a first mode of operation that emulates a local, non-cache memory and a second mode of operation that emulates a cache,

wherein a selection of any of the first mode of operation and the second mode of operation is capable of being overridden by another selection of an other of the first mode of operation and the second mode of operation.

27. The data system of claim 26, wherein the at least one microprocessor and the configurable memory array are integrated on a single chip.

28. The data system of claim 26, wherein the at least one microprocessor and the configurable memory array are integrated in a single package.

29. A memory system on a chip, comprising:

a processor; and

a configurable memory having three modes of operation, a first mode of operation for emulating a local, non-cache memory, a second mode of operation for emulating a cache, and a third mode of operation for emulating both the local memory and the cache, wherein any of the three modes of operation may be selected at any given time.

30. A method for accessing data, comprising the steps of:

providing a configurable memory on a chip;

providing control logic on the chip for selecting between a first mode of operation and a second mode of operation of the configurable memory and for overriding a

previous selection of the first mode of operation or the second mode of operation;

configuring the configurable memory as a local, non-cache memory in the first mode of operation;

configuring the configurable memory as a cache in the second mode of operation; and

accessing the data from the configurable memory, based upon a mode of the configurable memory.

31. The method of claim 30, further comprising the steps of:

providing at least one microprocessor for servicing memory access instructions for the configurable memory; and

integrating the at least one microprocessor with the configurable memory on the chip.

32. The method of claim 30, wherein the chip comprises a single chip.

33. A method for accessing data, comprising the steps of:

providing a configurable memory in a package;

providing control logic in the package for

selecting between a first mode of operation and a second mode of operation of the configurable memory and for overriding a previous selection of the first mode of operation or the second mode of operation;

configuring the configurable memory as a local, non-cache memory in the first mode of operation;

configuring the configurable memory as a cache in the second mode of operation; and

accessing the data from the configurable memory, based upon a mode of the configurable memory.

34. The method of claim 33, further comprising the steps of:

providing at least one microprocessor for servicing memory access instructions for the configurable memory; and

integrating the at least one microprocessor with the configurable memory in the package.

35. The method of claim 34, wherein said integrating step integrates the at least one microprocessor with the configurable memory based upon a chip stack technique.

36. The method of claim 34, wherein said integrating step integrates the at least one microprocessor with the configurable memory based upon a flip chip technique.

37. The method of claim 34, wherein said integrating step integrates the at least one microprocessor with the configurable memory based upon a multi-chip module.